AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (New) A semiconductor device made by providing on a substrate an active region that functions as a portion of an active element, wherein the active region is configured by alternately layering:

first semiconductor layers provided in plurality which function as a carrier transit region, and

second semiconductor layers, which are composed of δ doped layers provided in plurality, which include a higher concentration of impurities for carriers than

the first semiconductor layers, and which have a thinner film thickness than the first semiconductor layers,

wherein the first semiconductor layers and the second semiconductor layers are made of the same material,

wherein each of the first semiconductor layers has the same thickness within a range between 10nm and 100nm, and

wherein the concentration of impurities for carriers included in the second semiconductor layers is substantially constant.

14. (New) The semiconductor device according to claim 13, wherein the concentration of the carriers varies, such that the peak, which is the largest concentration of the carriers, is provided in the first semiconductor layers and the valley, which is the smallest concentration of the carriers, is provided in the second semiconductor layers.

15. (New) The semiconductor device according to claim 13, wherein the carriers exist not only in the first semiconductor layers but also in the second semiconductor layers.

16. (New) The semiconductor device according to claim 15, wherein the carriers are patterned from the first semiconductor layers to the second semiconductor layers.

17. (New) The semiconductor device according to claim 13, wherein the first semiconductor layers and the second semiconductor layers are made of one material selected from SiC, GaN, and GaAs.

18. (New) The semiconductor device according to claim 17, wherein the first semiconductor layers and the second semiconductor layers are made of SiC.

19. (New) The semiconductor device according to claim 13,

wherein the concentration of impurities for carriers in the first semiconductor layers is below $1*10^{17}$ atoms/cm^3, and

wherein the concentration of impurities for carriers in the second semiconductor layers is at least $1*10^{17}$ atoms/cm^3.

20. (New) The semiconductor device according to claim 13,

wherein the substrate is a semiconductor layer that includes a high concentration of impurities,

wherein the uppermost portion of the active region is made of the first semiconductor layers, and

wherein the semiconductor device further comprises:

a Schottky electrode providing a Schottky contact with a portion of the upper surface of the first semiconductor layers at the uppermost portion of the active region, and

an ohmic electrode providing an ohmic contact with a portion of the substrate.

21. (New) The semiconductor device according to claim 13,

wherein the uppermost portion of the active region is made of the first semiconductor layers, and

wherein the semiconductor device further comprises:

a Schottky gate electrode, which is in Schottky contact with a portion of the upper surface of the first semiconductor layers at the uppermost portion of the active region, and

source and drain electrodes, which are provided on the active region and sandwich the Schottky gate electrode, and which are connected to the active region.

22. (New) The semiconductor device according to claim 13, further comprising:

two third semiconductor layers, which are provided on the active region and sandwich the Schottky gate electrode, and which include a high concentration of impurities, and

wherein the source and drain electrodes are in ohmic contact with the third semiconductor layers.